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(54) **COMPLEMENTARY METAL-OXIDE SILICON HAVING SILICON AND SILICON GERMANIUM CHANNELS**

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See application file for complete search history.

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(57) **ABSTRACT**

A silicon germanium on insulator (SGOI) wafer having nFET and pFET regions is accessed, the SGOI wafer having a silicon germanium (SiGe) layer having a first germanium (Ge) concentration, and a first oxide layer over nFET and pFET and removing the first oxide layer over the pFET. Then, increasing the first Ge concentration in the SiGe layer in the pFET to a second Ge concentration and removing the first oxide layer over the nFET. Then, recessing the SiGe layer of the first Ge concentration in the nFET so that the SiGe layer is in plane with the SiGe layer in the pFET of the second Ge concentration. Then, growing a silicon (Si) layer over the SGOI in the nFET and a SiGe layer of a third concentration in the pFET, where the SiGe layer of a third concentration is in plane with the grown nFET Si layer.

6 Claims, 12 Drawing Sheets